

WHAT IS CLAIMED IS:

1. A self orthogonal decoding circuit performing decoding for self orthogonal code repeating decoding for said self orthogonal code for a plurality of times.

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2. A self orthogonal decoding circuit performing decoding for self orthogonal code on the basis of syndrome bit determined only by an error in a reception series which is generated by adding error to a transmission series which is in turn generated by parallel/serial conversion with adding an check series to
10 an information series, comprising:

a plurality of stages of deciding circuit for repeating decoding for said self orthogonal code for a plurality of times;
and

15 check series register provided for each of decoding circuit except for the decoding circuit at a final stage among said plurality of stages of decoding circuits and for inputting said check series to next stage of decoding circuit with delay.

20 3. A self orthogonal decoding circuit as set forth in claim 2, wherein, in said plurality of stages of decoding circuits, a threshold value judgment threshold value for making judgment as error in first decoding is set large to make correction only for high probability of error being corrected, and said threshold
25 value judgment threshold value being gradually reduced as

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repeated decoding for said self orthogonal code, for making correction for lower probability of error.

4. A self orthogonal decoding circuit as set forth in claim 2, which comprises means for performing code synchronization judgment by counting number of errors as being judged as error and performing code synchronization on the basis of counted error number.

10 5. A self orthogonal decoding circuit as set forth in claim 3, which comprises code synchronization dedicated threshold value judgment circuit provided separately from the circuit for making judgment of said error and dedicated for code synchronization and making judgment whether error is caused
15 or not on the basis of threshold value judgment threshold value optimized for code synchronization and said threshold value of said code synchronization dedicated threshold value judgment circuit to be lower than said threshold value judgment threshold value.

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6. A self orthogonal decoding circuit as set forth in claim 5, which comprises a syndrome register which shifts said syndrome bit provided for code synchronization to output to said code synchronization dedicated threshold value judgment circuit,
25 so as not to perform correction on the basis of the result of

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error judgment of said code synchronization dedicated threshold value judgment circuit for said syndrome register.

7. A self orthogonal decoding circuit as set forth in claim 4, wherein each decoding circuit in said plurality stages comprises:

syndrome generation means for generating said syndrome bit;

error value generation means for leading an error value by making judgment of error of said syndrome bit generated by said syndrome generation means on the basis of said threshold value judgment threshold value;

error correcting means for correcting error of said syndrome bit on the basis of said error value generated by said error value generation means; and

error detection counter for counting said error number on the basis of said error value generated by said error value generation means.

8. A self orthogonal decoding circuit as set forth in claim 1, wherein, in a system including an information source generating an information series, an encoder for converting said information series into a code series, and a communication path for transmitting said code series, decoding for said self orthogonal code is repeated for a plurality of times.

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9. A self orthogonal decoding circuit as set forth in claim 8, wherein said communication path is constructed with a wired cable.

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10. A self orthogonal decoding circuit as set forth in claim 9, wherein said wired cable is an optical cable.

11. A self orthogonal decoding circuit as set forth in claim 10 8, wherein said communication path is a transmission path in radio communication.

12. A self orthogonal decoding method for performing decoding for self orthogonal code repeating decoding for said self 15 orthogonal code for a plurality of times.

13. A self orthogonal decoding method performing decoding for self orthogonal code on the basis of syndrome bit determined only by an error in a reception series which is generated by 20 adding error to a transmission series which is in turn generated by parallel/serial conversion with adding an check series to an information series, comprising a step of:

in each of a plurality of stages of deciding circuit for repeating decoding for said self orthogonal code for a plurality 25 of times, said check series being input to next stage of decoding

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circuit with a delay except for the decoding circuit at the final stage.

14. A self orthogonal decoding method as set forth in claim
5 13, wherein, in said plurality of stages of decoding circuits,
a threshold value judgment threshold value for making judgment
as error in first decoding is set large to make correction only
for high probability of error being corrected, and said threshold
value judgment threshold value being gradually reduced as
10 repeated decoding for said self orthogonal code, for making
correction for lower probability of error.

15. A self orthogonal decoding method as set forth in claim
13, which comprises means for performing code synchronization
15 judgment by counting number of errors as being judged as error
and performing code synchronization on the basis of counted
error number.

16. A self orthogonal decoding method as set forth in claim
20 15, wherein a threshold value of a code synchronization dedicated
threshold value judgment circuit provided separately from the
circuit for making judgment of said error and dedicated for
code synchronization and making judgment whether error is caused
or not on the basis of threshold value judgment threshold value
25 optimized for code synchronization, being set lower than said

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threshold value judgment threshold value.

17. A self orthogonal decoding method as set forth in claim
16, which comprises a step of providing a syndrome register
5 which shifts said syndrome bit provided for code synchronization
to output to said code synchronization dedicated threshold value
judgment circuit, so as not to perform correction on the basis
of the result of error judgment of said code synchronization
dedicated threshold value judgment circuit for said syndrome
10 register.

18. A self orthogonal decoding method as set forth in claim
15, which includes
step of generating said syndrome bit,
15 step of leading an error value by making judgment of error
of said syndrome bit generated by said syndrome generation means
on the basis of said threshold value judgment threshold value,
step of correcting error of said syndrome bit on the basis
of said error value generated by said error value generation
20 means; and

step of counting said error number on the basis of said
error value generated by said error value generation means.

19. A self orthogonal decoding method as set forth in claim
25 12, wherein, in a system including an information source

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generating an information series, an encoder for converting said information series into a code series, and a communication path for transmitting said code series, decoding for said self orthogonal code is repeated for a plurality of times.

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20. A self orthogonal decoding method as set forth in claim 19, wherein said communication path is constructed with a wired cable.

10 21. A self orthogonal decoding method as set forth in claim 20, wherein said wired cable is an optical cable.

22. A self orthogonal decoding method as set forth in claim 19, wherein said communication path is a transmission path in
15 radio communication.

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